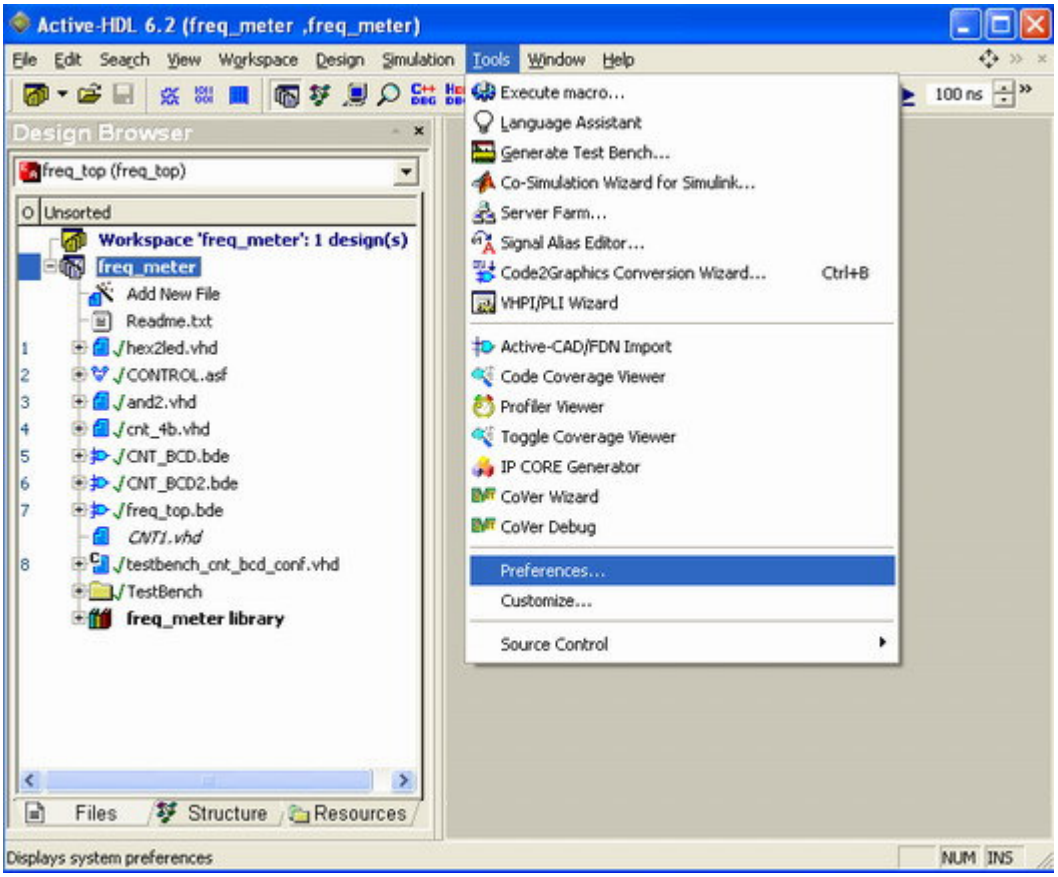
Using Active-HDL with Xilinx ISE 6.2

Introduction

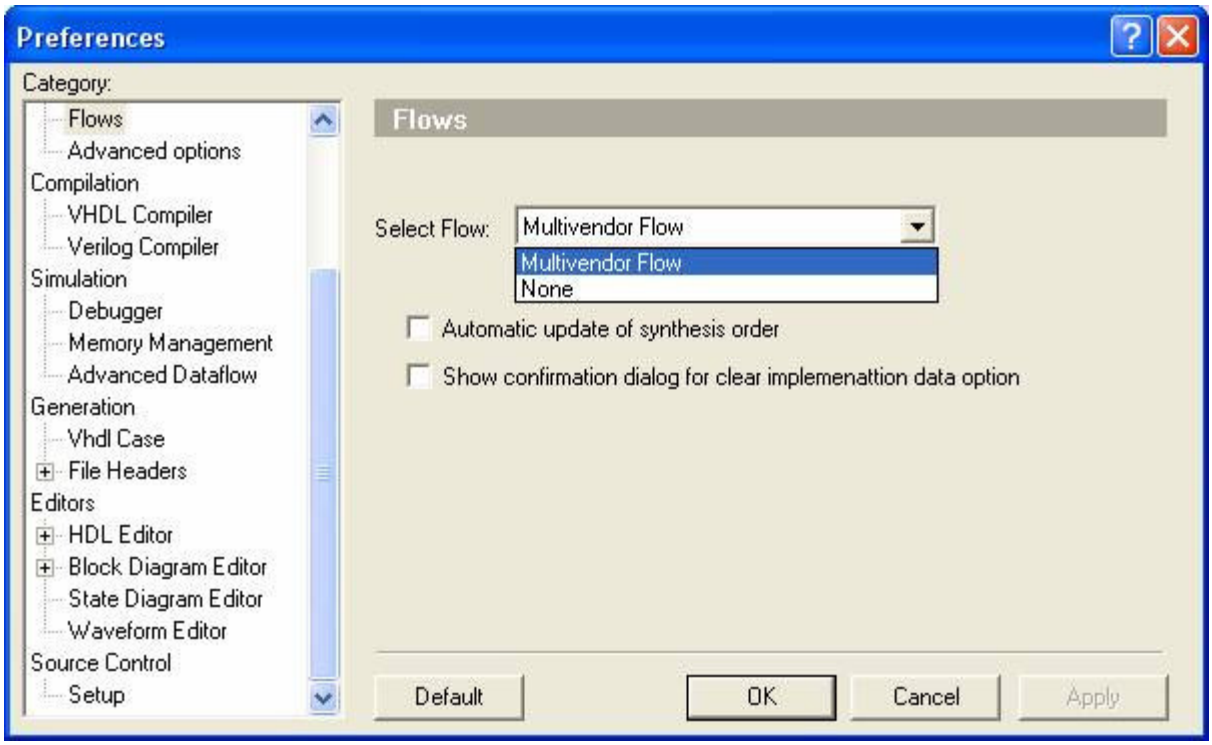
To offer a complete design environment for Xilinx* users, Aldec has developed a TCL script that automates the design flow between Aldec's Active-HDL and Xilinx's Xilinx ISE*.
This application note is divided into the following three sections:

1. The Flow Configuration Settings window.
2. Running Synthesis.
3. Running Implementation.

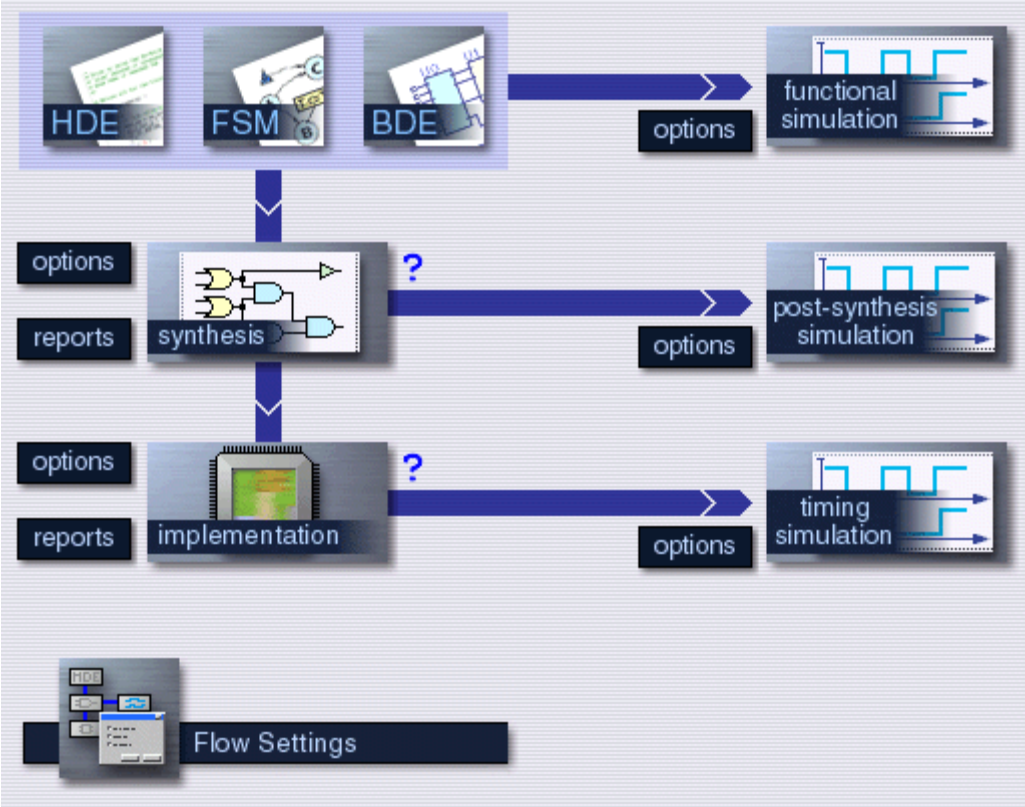
Procedures



With a design opened and displayed in the Design Browser as shown in the figure above, go to the **Tools** menu and select the **Preferences** option. In the **Preferences** window, select the category Environment → Flows. In the "Select Flow" dialog box, select the **Multivendor Flow** option. Click on the Apply button, and then click on the OK button.

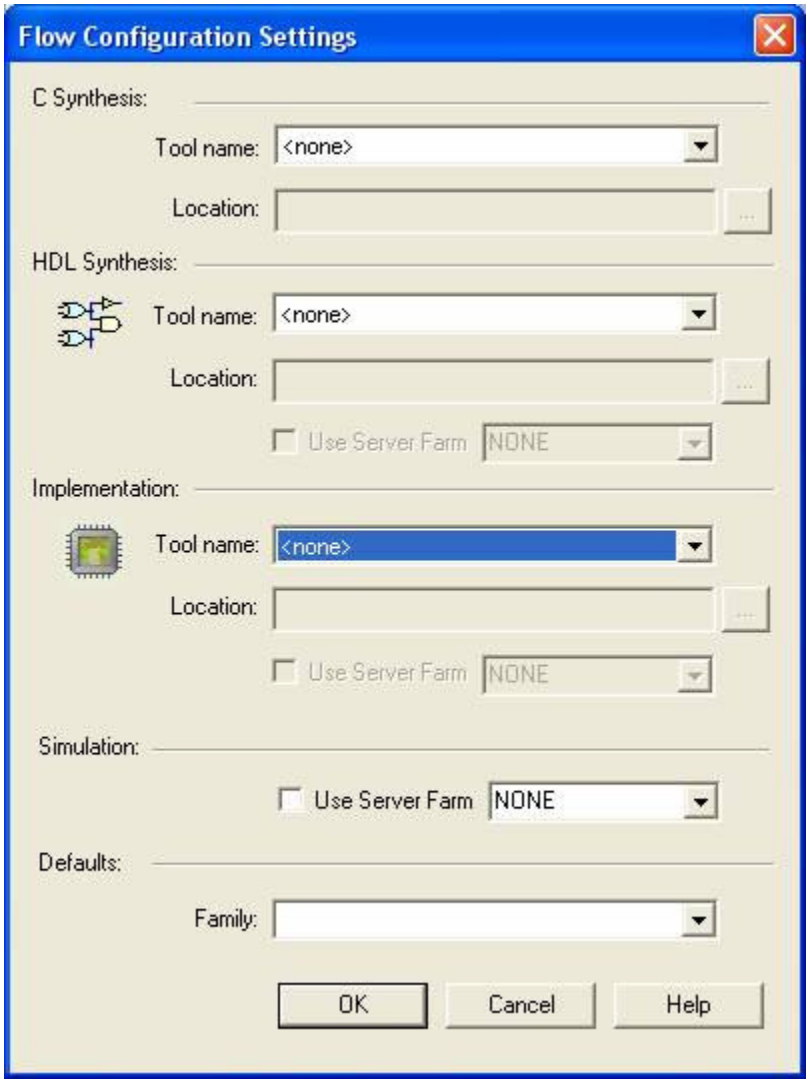


Selecting the **Multivendor Flow** will give you the option to choose the desired Synthesis Tool and Implementation Tool, Xilinx ISE later in the **Flow Settings** window. But first, you must open the **Design Flow Manager**. To open the Design Flow Manager, simply click on its icon  in the standard toolbar.

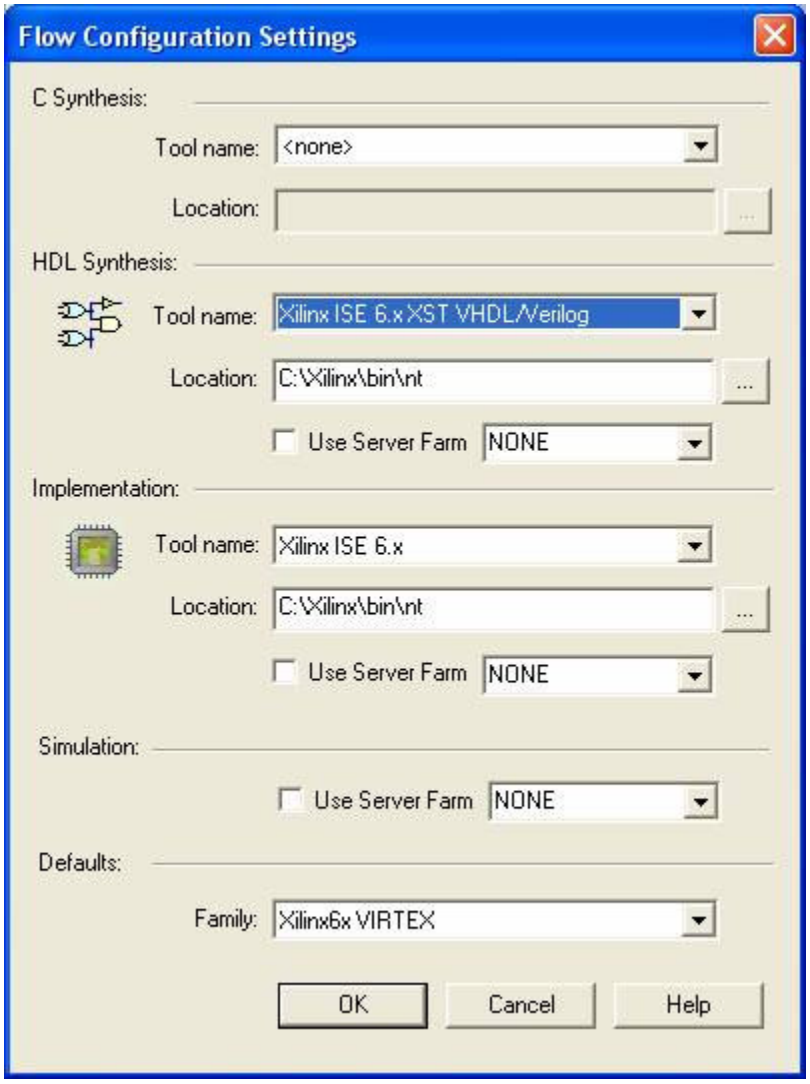


The Flow Configuration Settings window

When opening the Design Flow Manager for the first time, the **Flow Settings** window must be configured. Click on the **Flow Settings** button in the Design Flow Manager, the following window will be invoked.



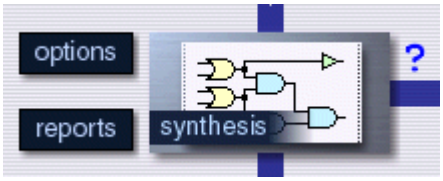
In the **Flow Configuration Settings** window, you will specify which Synthesis and Implementation Tool you would like to use to perform Synthesis and Implementation, respectively. By default, the Synthesis and Implementation Tools are set to . You can then select the desired Synthesis Tool and Implementation Tool, Xilinx ISE. When you make a selection, the location for the (.exe) file can be automatically located by Active-HDL or you can specify the location manually. This allows Active-HDL to run the tool in batch/GUI mode.
The Flow Configuration Settings window with Xilinx ISE selected as Synthesis and Implementation Tool, respectively, is shown below.



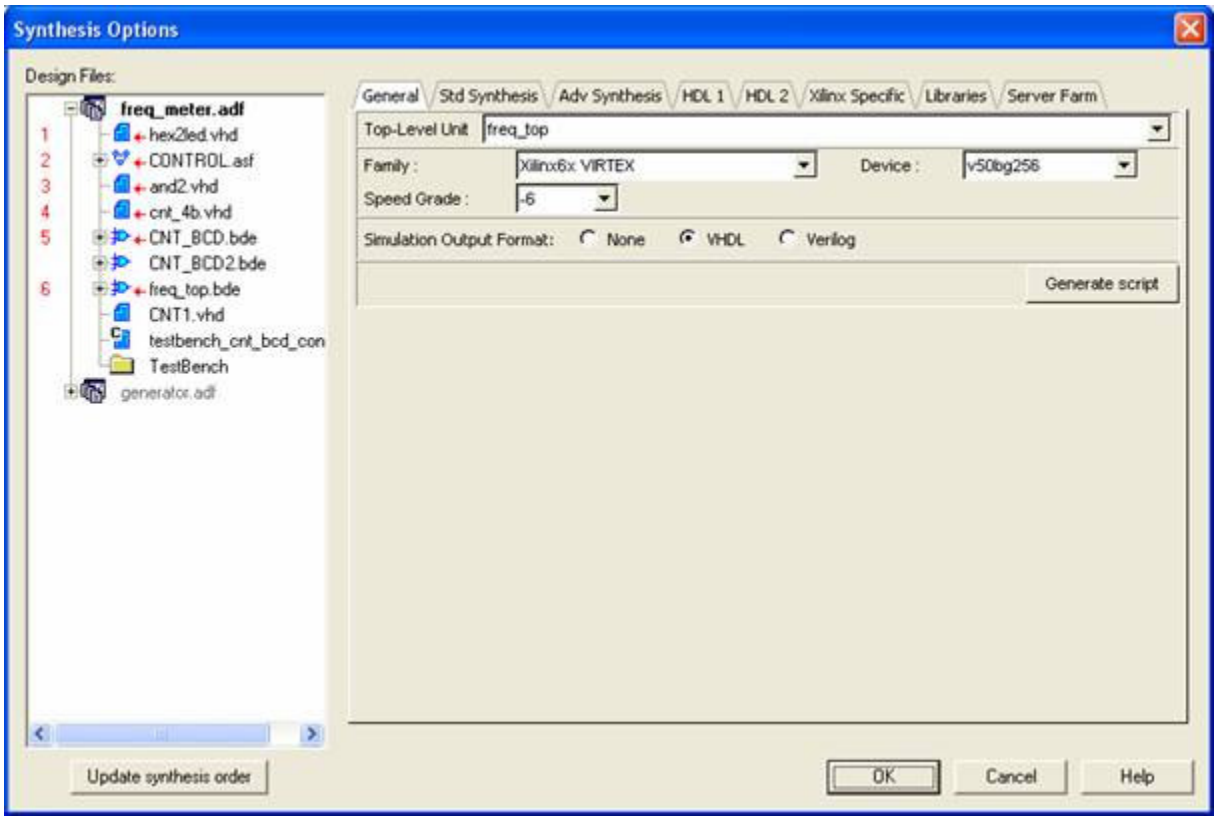
After selecting the desired Synthesis and Implementation Tool, the option to use Server Farm for synthesis and implementation is automatically added. Additionally, you can also select the option to use Server Farm for Simulation. In the lower part of the window, you can select the Family of Xilinx devices.

Running Synthesis

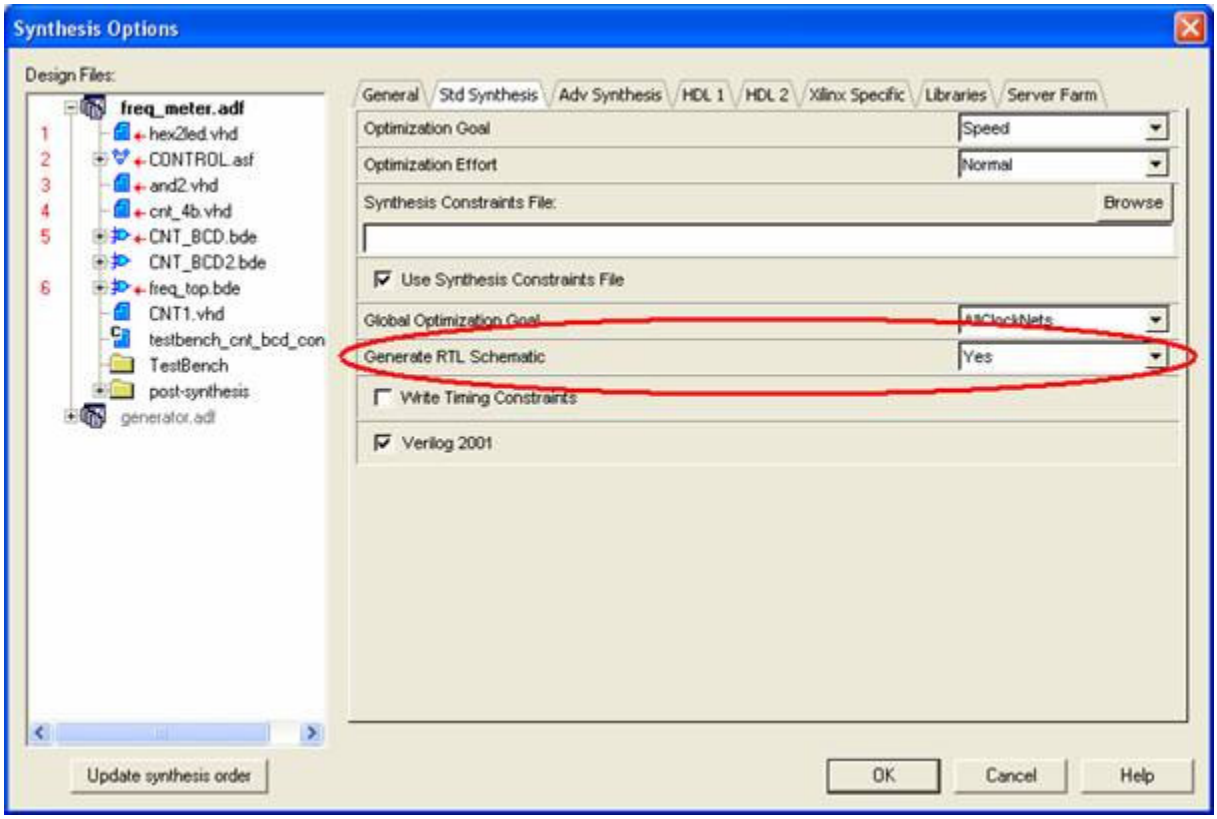
After RTL simulation has been completed in Active-HDL, the files can be passed to Synthesis. Synthesis settings can be configured with the Synthesis **options** button in the Design Flow Manager.



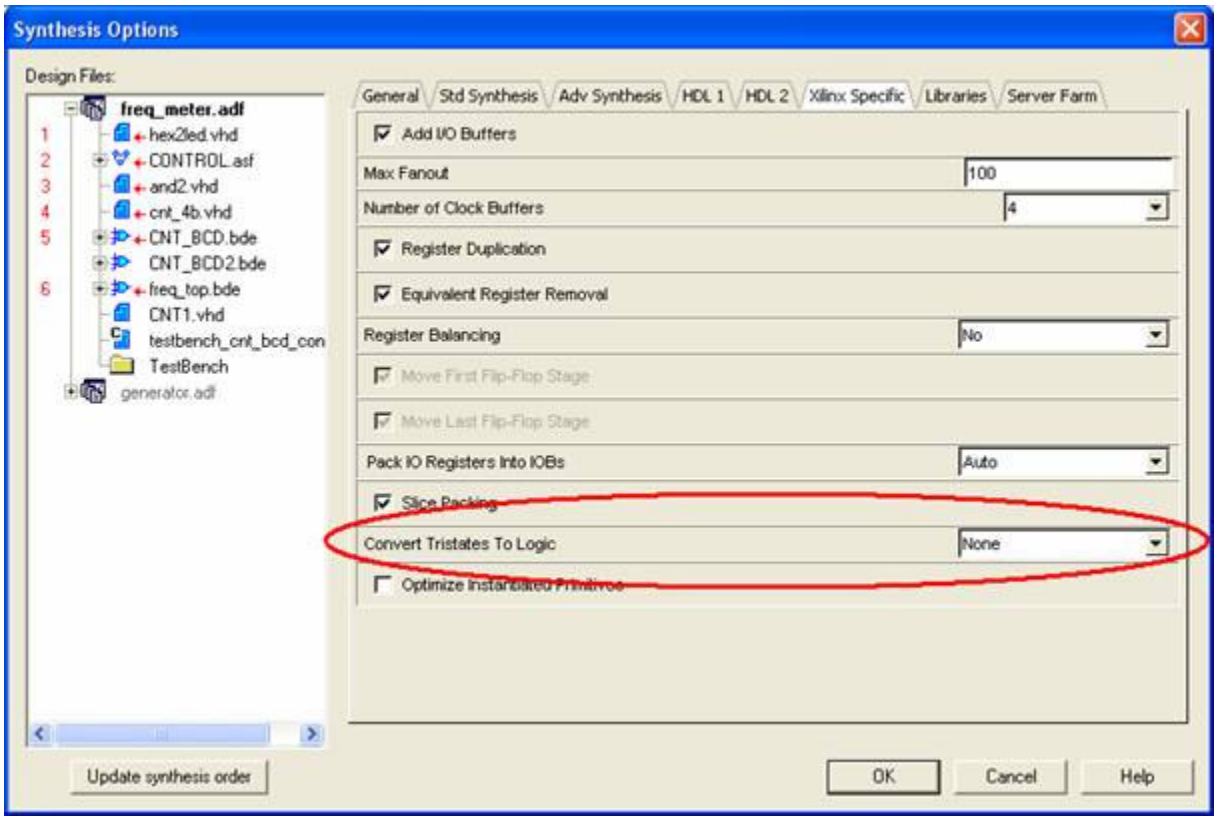
Clicking on the Synthesis **options** button invokes the following window.



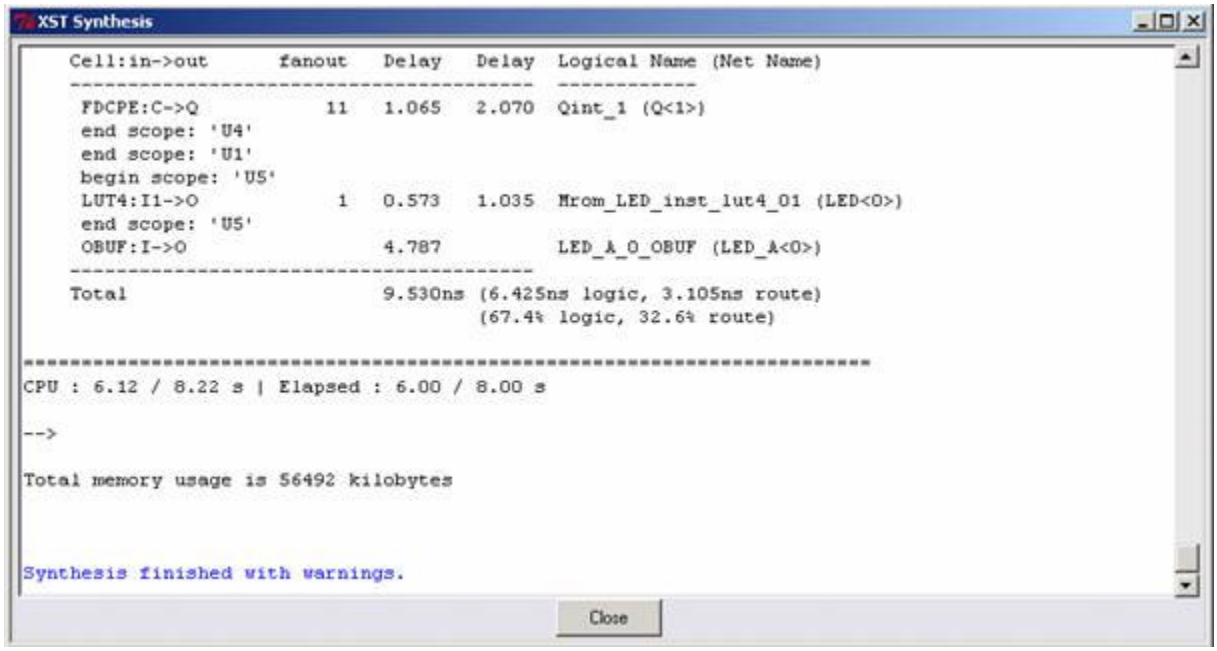
In this window, you can specify the Synthesis settings: which files should be taken to Synthesis, which file should be selected as the top level, frequency settings and more. Additionally, clicking on the drop-down dialog box, gives you the option to select the desired Xilinx Family of devices. When the proper Family is chosen, in the **Device** drop down box, you can find only devices that correspond to this family; this means that the drop down box is updated based on the chosen family. Also, in this window you can designate whether Synthesis will be run in GUI or batch mode. To view RTL schematic available after synthesis please choose “YES” for the Generate RTL schematic in options tab “std synthesis” under the synthesis options as shown below:



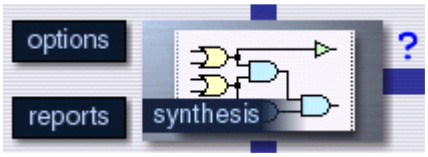
NOTE: If synthesis is run in batch mode, Active-HDL takes full control of the process. This means that all settings and files will be automatically passed to the Synthesis tool and when Synthesis is complete all results from the Synthesis Tool will be passed to Active-HDL. If the Synthesis tool is run in GUI mode, Active-HDL passes all necessary design files to the Synthesis tool, but the user will need to transfer the results from Synthesis back to Active-HDL in order to be passed to Implementation or for gate level simulation.
NOTE: While running synthesis in Active-HDL 6.2 sp1 with Xilinx ISE 6.1 or higher make sure the option “convert Tristate to logic” is set to “none” as shown below:



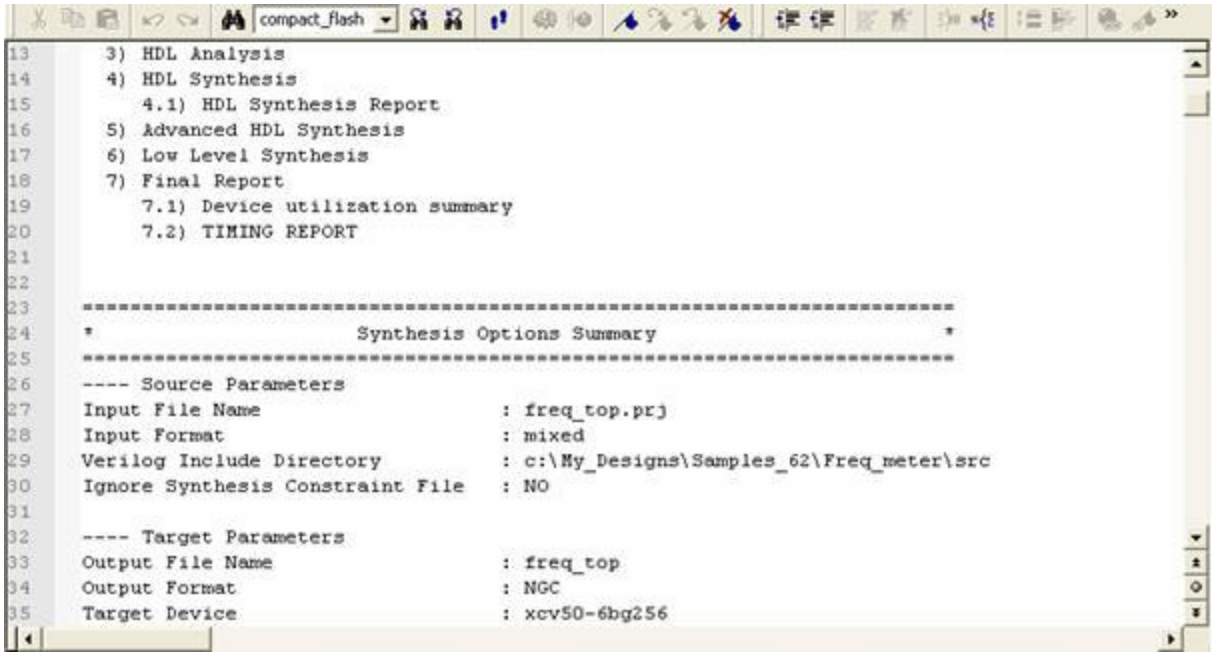
Once the Synthesis options are set, the user can automatically perform push-button Synthesis by clicking on the **synthesis** button in the Design Flow Manager. When Synthesis is run in batch mode, all Synthesis results and information can be seen on-line in a special window as shown below:



NOTE: This window can be minimized during synthesis and Active-HDL still can be used during this time.
Synthesis reports can then be viewed by clicking on the corresponding Synthesis **reports** button in the Design Flow Manager.



Clicking on the **reports** button invokes the following window.



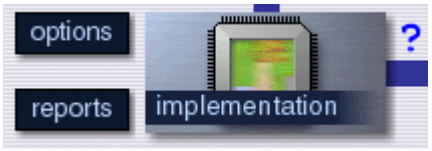
Choosing the **Synthesis Log** for example, invokes an HTML report as shown below:

When synthesis is successfully completed, a check mark is displayed next to the button in the flow menu. The file created after synthesis using Xilinx's XST is in .ngc file format. Below, is a list of the other marks that might appear in the flow chart during Synthesis and Implementation:

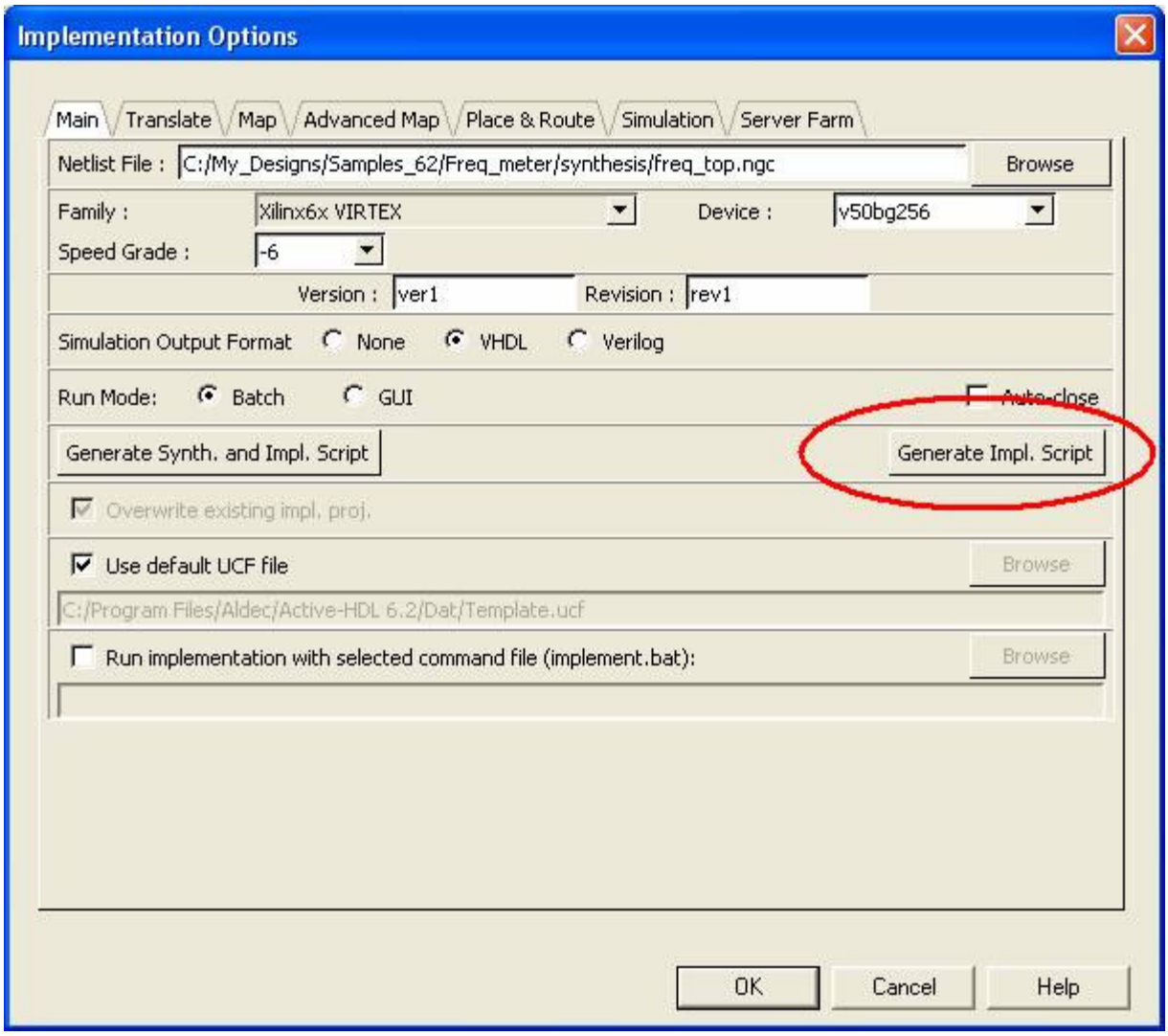
1.**!** there are warnings and can be viewed in the log file
2.**?** Need to update the operation
3.√ no errors and no warnings.
4.**X** some errors have accorded view the log file

Running Implementation

To run the Xilinx ISE Implementation Tool, the same steps need to be taken as for Synthesis. Clicking on the implementation **options** button in the Design Flow Manager also allows users to configure the settings.

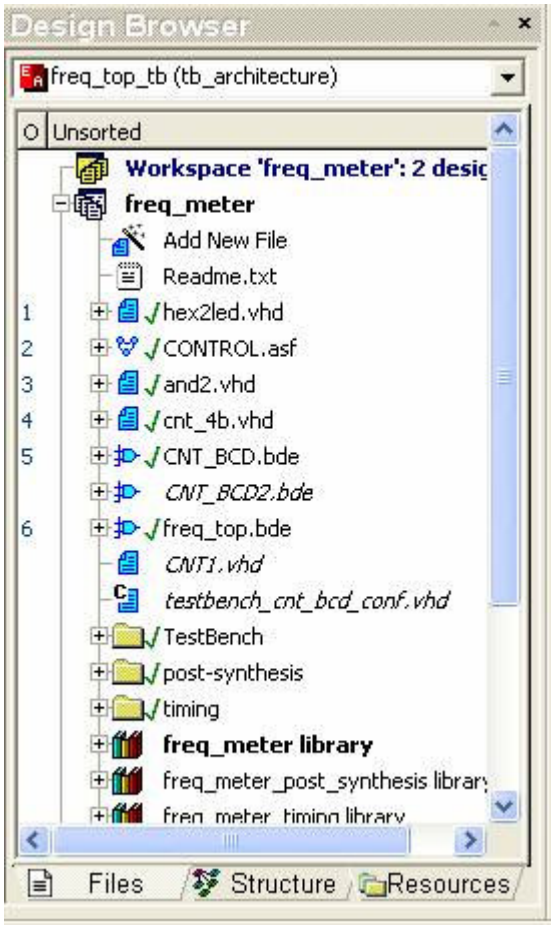


Because both Synthesis and Implementation processes are integrated in Active-HDL, by default, the Implementation settings are made based on the Synthesis settings. This means that Active-HDL knows the top-level netlist, family and device for Implementation based on the settings made in the Synthesis options window. If these settings are appropriate, when Synthesis is done, click on the **implementation** button in the Design Flow Manager to run Implementation in batch mode. Tcl scripts can also be generated automatically by clicking on the Generate implementation scripts option and specifying a file name for the script as shown below:



The **Xilinx ISE Implementation** window will be invoked, showing all messages from the Implementation tool.

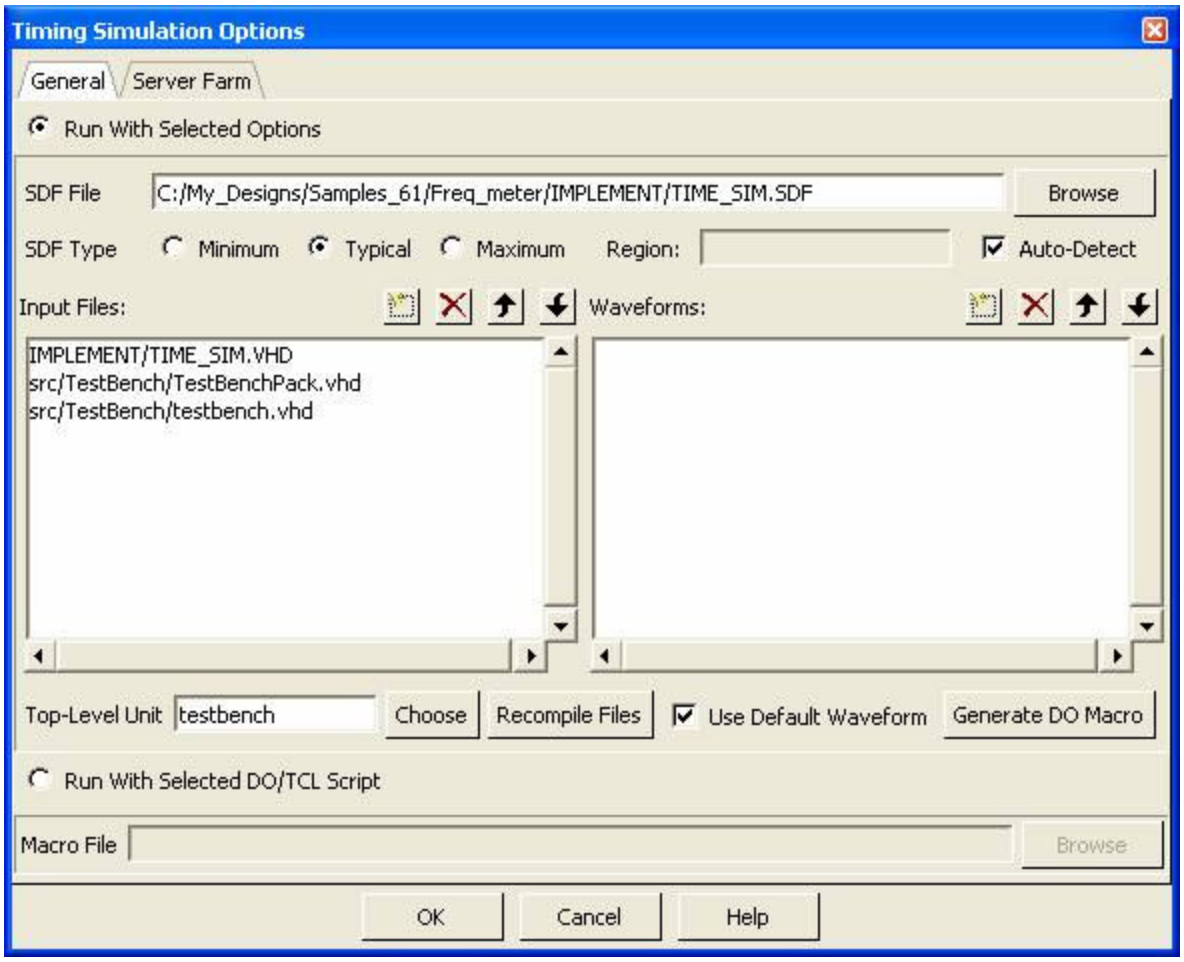
When implementation is completed, a subfolder labeled **Timing** is added to the Active-HDL Design Browser window. This folder contains all the necessary files to perform timing simulation (VHDL or Verilog) including the SDF file.



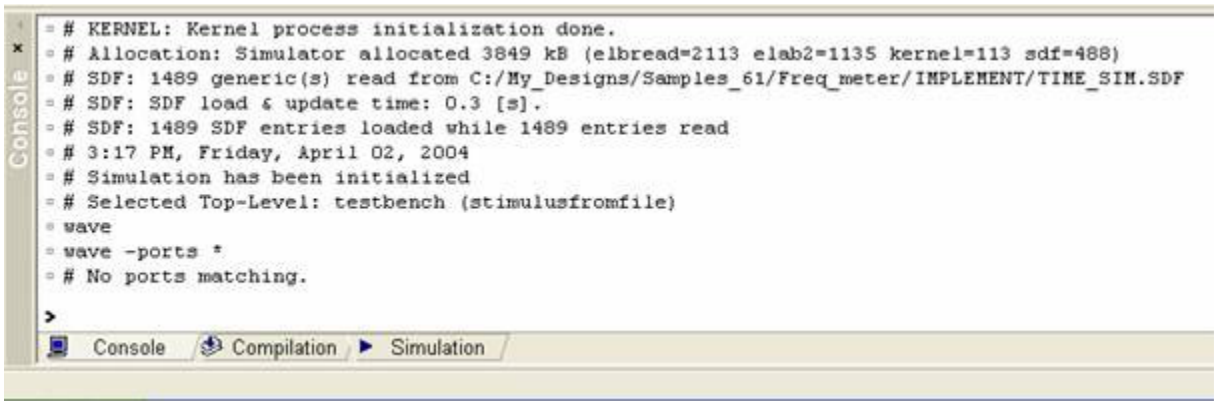
The files generated by the implementation tool can be used for timing simulation. Timing simulation can be run directly from the Design Flow Manager using the **timing simulation** button.

To view RTL Shematic available after synthesis (or) Static Timing analysis after place and route please click on the appropriate icon under design flow manager:

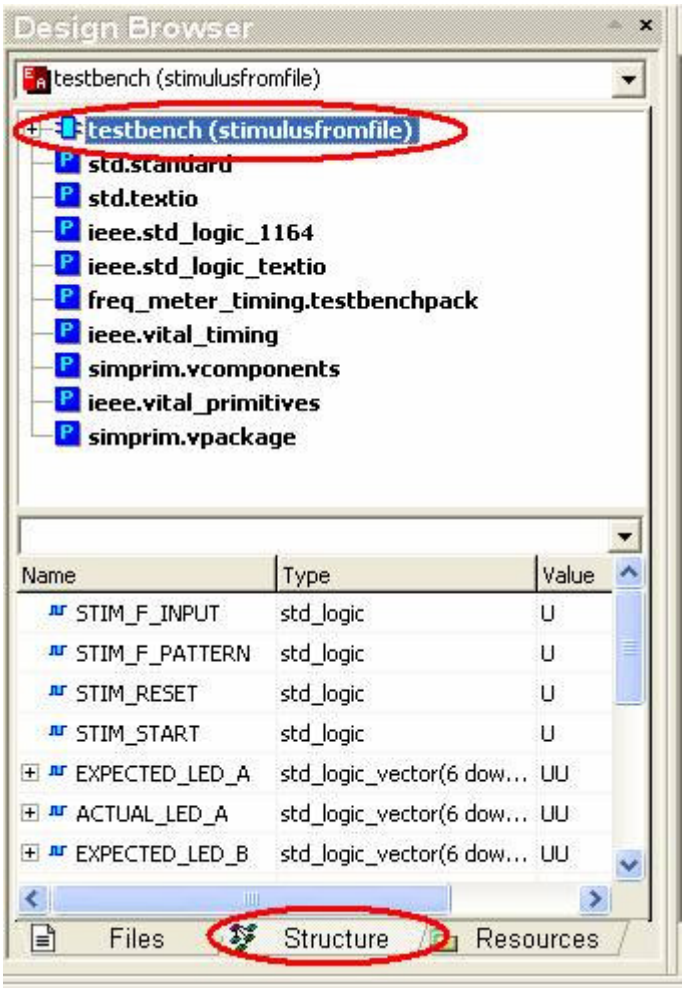
Note that the settings for timing simulation must be configured first, you can do this by clicking on its corresponding **options** button. For a more detailed description of the timing simulation procedures, refer to app note titled “Timing Simulation in Active-HDL”.



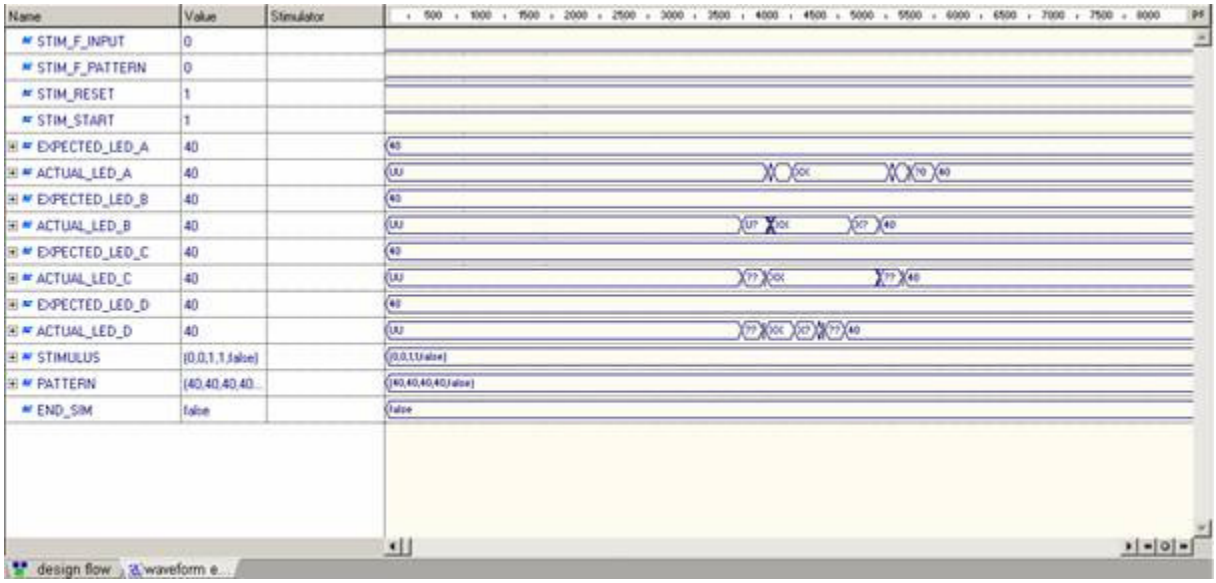
Choose the .SDF file and .vhd file generated after implementation as chosen in the diagram. Also choose a top-level unit. You can also choose the SDF type to be minimal, typical or maximum. After making your selections, click on the timing simulation icon in the design flow manager. Active-HDL will start compiling the design files and after simulation has been initialized you should be seeing the following message in your Active-HDL console:



After the simulation has been initialized, go to the structures tab of the design browser and select the freq_top_tb (tb_architecture) and drag the signals on to the new waveform window already created when the simulation is initialized.



After adding all the signals you need from the structures tab, run the simulation for a specific time interval  and check the simulation results in the waveform as shown below:



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